Solutions - Midterm Exam

(October 18th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

a) Complete the following table. The decimal numbers are unsigned: (5 pts.)

Decimal	BCD	Binary	Reflective Gray Code
37	00110111	100101	110111
162	000101100010	10100010	11110011
69	01101001	1000101	1100111

b) Complete the following table. Use the fewest number of bits in each case: (12 pts.)

REPRESENTATION				
Decimal	Sign-and-magnitude	1's complement	2's complement	
-63	1111111	1000000	1000001	
-16	110000	101111	10000	
-11	11011	10100	10101	
29	011101	011101	011101	
-32	1100000	1011111	100000	
0	00	11111	0	

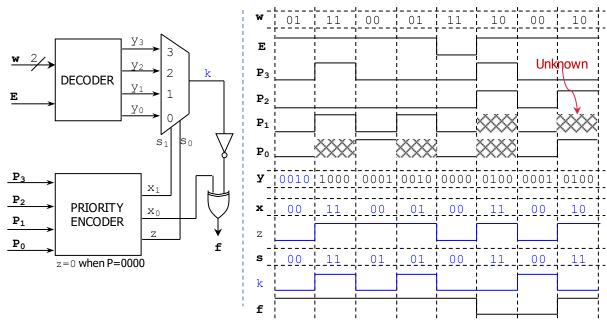
c) Convert the following decimal numbers to their 2's complement representations. (3 pts) 17.875 ✓ -16.3125

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+17.875 = 010001.111
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+16.3125 = 010000.0101
\Rightarrow -16.3125 = 101111.1011
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PROBLEM 2 (15 PTS)

• Complete the timing diagram of the circuit shown below. $y = y_3 y_2 y_1 y_0$, $x = x_1 x_0$, $s = s_1 s_0$



PROBLEM 3 (17 PTS)

a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every carry (or borrow) from c_0 to c_n (or b_0 to b_n). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte. (6 pts)

✓ 51 + 15

✓ 22 - 33

 $b_{0}^{1}=0$ $b_{1}^{1}=0$ b_{1 **c₆=1** c₅=1 c₅=1 c₄=1 c₃=1 c₁=1 c₁=1 c₁=0 c₀=0 Borrow out! -1 1 0 0 1 1 + $51 = 0 \times 33 =$ $22 = 0 \times 16 = 0 1 0 1 1 0 15 = 0 \times 0F =$ 0 0 1 1 1 1 $33 = 0 \times 21 = 1 \ 0 \ 0 \ 0 \ 1$ Overflow! 1000010 1 1 0 1 0 1 b) Perform the following operations, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n . For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts) ✓ -61 - 18 41 + 24 $C_{6}=0$ $C_{5}=0$ $C_{4}=1$ $C_{4}=1$ $C_{3}=1$ $C_{3}=1$ $C_{2}=1$ $C_{1}=0$ $C_{0}=0$ c₄=1 c₃=0 $c_2=0$ $c_1=0$ $c_0=0$ n = 7 bits c5=1 Ľ, C.61 n = 7 bits 41 = 0 1 0 1 0 0 1 + $C_7 \oplus C_6 = 1 - 61 = 1 1 0 0 0 0 1 1 +$ c₇⊕c₆=0 Overflow! -18 = 1 1 1 0 1 1 1 0 24 = 0 0 1 1 0 0 0No Overflow 0110001 1000001 $-61 - 18 = -79 \notin [-2^{6}, 2^{6} - 1] \rightarrow \text{overflow}!$ $41 + 24 = 65 \notin [-2^6, 2^{6}-1] \rightarrow \text{overflow}!$ To avoid overflow: n = 8 bits (sign-extension) To avoid overflow: n = 8 bits (sign-extension) c₈⊕c₇=0 $c_{6}=0$ $c_{5}=0$ $c_{4}=1$ $c_{3}=1$ **C₆=1 C₅=1 C₄=1** $c_3=0$ $c_2=0$ $c_1=0$ $c_0=0$ $c_2 = 1$ $c_1 = 0$ C₀=0 <u>[</u>] 511 0<u>1</u>0 No Overflow -61 = 1 1 0 0 0 0 1 1 + $41 = 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \ +$ C₈⊕C₇=0 -18 = 1 1 1 0 1 1 1 024 = 0 0 0 1 1 0 0 0No Overflow 1 0 1 1 0 0 0 1 65 = 0 1 0 0 0 0 1 $-61 - 18 = -79 \in [-2^7, 2^7 - 1] \rightarrow \text{no overflow}$ $41 + 24 = -65 \in [-2^7, 2^7-1] \rightarrow \text{no overflow}$ c) Perform binary multiplication of the following numbers that are represented in 2's complement arithmetic with 4 bits. (3 pts) ✓ -7 x 6. 1001x 0 1 1 1 x 0 1 1 0 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 0 0 0 0

PROBLEM 4 (10 PTS)

The figure below depicts the entire memory space of a microprocessor. Each memory address occupies one byte. 1KB = 2¹⁰ bytes, 1MB = 2²⁰ bytes, 1GB = 2³⁰ bytes

1 0 1 0

1010110

✓ What is the size (in bytes, KB, or MB) of the memory space? What is the address bus size of the microprocessor? (2 pts.)

Address space: 0×00000 to $0 \times FFFFF$. To represent all these addresses, we require 20 bits. So, the address bus size of the microprocessor is 20 bits. The size of the memory space is then $2^{20} = 1$ MB.

✓ If we have a memory chip of 128 KB, how many bits do we require to address those 128 KB of memory? (1 pt.)

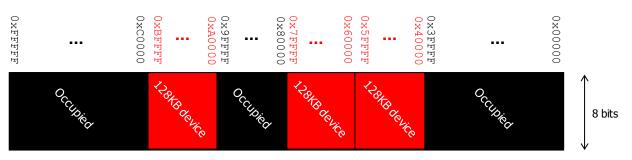
128 KB memory device: 128KB = 2^{17} bytes. Thus, we require 17 bits to address the memory device.

0 1 0

✓ We want to connect the 128 KB memory chip to the microprocessor. For optimal implementation, we must place those 128 KB in an address range where every address shares some MSBs. Provide a list of all the possible address ranges that the 128 KB memory chip can occupy. You can only use the non-occupied portions of the memory space as shown below.

 ^o 0x40000 to 0x5FFFF

 ^o 0x60000 to 0x5FFFF



2

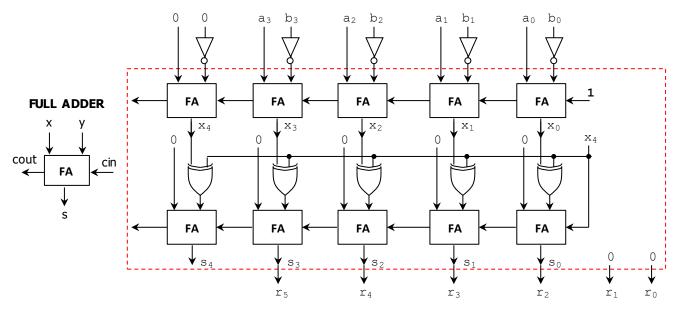
PROBLEM 5 (10 PTS)

• Sketch the circuit that computes $|A - B| \times 4$, where A, B are 4-bit <u>unsigned</u> numbers. For example: $A = 0101, B = 1101 \rightarrow |A - B| \times 4 = 8 \times 4 = 32$. You can only use full adders and logic gates. Your circuit must avoid overflow.

 $A = a_3 a_2 a_1 a_0, B = b_3 b_2 b_1 b_0$

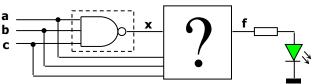
 $A, B \in [0,15] \rightarrow A, B$ require 4 bits in unsigned representation. However, to get the proper result of A - B, we need to use the 2C representation, where A, B require 5 bits in 2C.

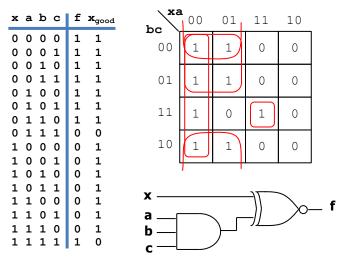
- \checkmark X = A B \in [-15,15] requires 5 bits in 2C. Thus, we need to zero-extend A and B to convert them to 2C representation.
- ✓ $|X| = |A B| \in [0,15]$ requires 5 bits in 2C. Thus, the second operation $0 \pm X$ only requires 5 bits.
 - If $x_4 = 1 \rightarrow X < 0 \rightarrow \text{we do } 0 X$.
 - If $x_4 = 0 \rightarrow X \ge 0 \rightarrow \text{we do } 0 + X$.
- ✓ $R = |A B| \times 4 \in [0,60]$ requires 7 bits in 2C. Note that the MSB is always 0. The unsigned result only requires 6 bits.



PROBLEM 6 (16 PTS)

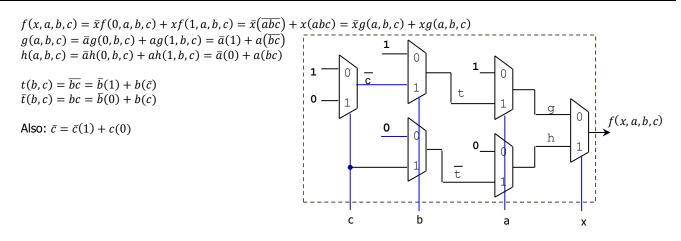
- We want to design a circuit that verifies the logical operation of a 3-input NAND gate. f = 1 (LED ON) if the NAND gate does NOT work properly (Assumption: when the NAND gate is not working, it generates 1's instead of 0's and vice versa).
 - ✓ Provide the Boolean equation for *f* and sketch the circuit using logic gates. (4 pts.)
 - Implement the circuit using <u>ONLY</u> 2-to-1 MUXs (AND, OR, NOT, XOR gates are not allowed). (12 pts)





 $f = \bar{x}\bar{b} + \bar{x}\bar{c} + \bar{x}\bar{a} + xabc = \bar{x}(\overline{abc}) + x(abc)$

$$f = \overline{x \oplus (abc)}$$



PROBLEM 7 (12 PTS)

• Complete the timing diagram of the following circuit. The VHDL code (tst.vhd) corresponds to the shaded circuit. $z = z_1 z_0$, $y = y_3 y_2 y_1 y_0$

